Electronic Version
Stylesheet Version v1.1.1

[REMOTE BIST FOR HIGH SPEED TEST AND REDUNDANCY CALCULATION]

Abstract

Disclosed is a hybrid built-in self test (BIST) architecture for embedded memory arrays that segments BIST functionality into remote lower-speed executable instructions and local higher-speed executable instructions. A standalone BIST logic controller operates at a lower frequency and communicates with a plurality of embedded memory arrays using a BIST instruction set. A block of higher-speed test logic is incorporated into each embedded memory array under test and locally processes BIST instructions received from the standalone BIST logic controller at a higher frequency. The higher-speed test logic includes a multiplier for increasing the frequency of the BIST instructions from the lower frequency to the higher frequency. The standalone BIST logic controller enables a plurality of higher-speed test logic structures in a plurality of embedded memory arrays.